Amendments to the Claims:

The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A semiconductor device with a negative voltage regulator comprising:

a negative voltage regulator capable of regulating a negative input voltage and outputting a negative output voltage at ~~an~~ a first output node, the negative voltage regulator comprising:

a driver for adjusting the negative output voltage, the driver comprising a first transistor and a second transistor, a first node and ~~an~~ a second output node, wherein the first node is electrically connected with a first voltage source and the second output node is electrically connected with the first output node of the negative voltage regulator;

a first operational amplifier comprising a first input end, a second input end and an output end electrically connected with a feedback voltage, a first reference voltage and the first transistor respectively, the first operational amplifier capable of outputting a driving voltage for controlling a current of the first transistor according to the feedback voltage and the first reference voltage;

a second operational amplifier comprising a first input end, a second input end and an output end electrically connected with a second reference voltage, the feedback voltage and the second transistor respectively, the second operational amplifier capable

of outputting a driving voltage for controlling a current of the second transistor according to the second reference voltage and the feedback voltage;

a current source circuit capable of providing the driver a current, the current source circuit comprising two triple-well n-type metal-oxide semiconductor (NMOS) transistors, wherein drains of the two triple-well NMOS transistors are electrically connected with a drain of the first transistor and a drain of the second transistor separately and sources of the two triple-well NMOS transistors are electrically connected with the negative input voltage; and

a voltage potential divider comprising a first end, a second end and a feedback node, wherein the first end and the second end are electrically connected with a second voltage source and the first output node respectively, and the feedback node is electrically connected with the first input end of the first operational amplifier and the second input end of the second operational amplifier, the voltage potential divider capable of generating the feedback voltage by dividing the potentials of the second voltage source and the negative output voltage and outputting the feedback voltage to the first operational amplifier and the second operational amplifier for adjusting the current of the first transistor and the current of the second transistor and thereby regulating the negative output voltage.

Claim 2 (original): The semiconductor device of claim 1 wherein each of the first transistor and the second transistor is a p-type metal-oxide semiconductor (PMOS) transistor.

Claim 3 (original): The semiconductor device of claim 1 wherein each of the first transistor and the second transistor is a PMOS transistor, wherein a source of the first transistor and a source of the second transistor are electrically connected with the first voltage source, a gate of the first transistor is electrically connected with the output end of the first operational amplifier and a gate of the second transistor is electrically connected with the output end of the secondoperational amplifier.

Claim 4 (currently amended): The semiconductor device of claim 3 wherein the second output node of the driver is the drain of the first transistor.

Claim 5 (currently amended): The semiconductor device of claim 3 wherein the second output node of the driver is the drain of the second transistor.

Claim 6 (currently amended): The semiconductor device of claim 1 wherein for each of the two triple-well NMOS transistors a base is electrically connected with ~~the~~ a source; the drain and a gate of one triple-well NMOS transistor are electrically connected with each other, and the drain of the other triple-well NMOS transistor is electrically connected with the second output node of the driver.

Claim 7 (original): The semiconductor device of claim 1 further comprising an oscillator and a negative pump, wherein an output end of the oscillator is electrically connected with an input end of the negative pump, and an output end of the negative pump is electrically connected with the sources of the two triple-well NMOS transistors.

Claim 8 (currently amended): The semiconductor device of claim 1 further comprising a reference voltage generator capable of generating the first reference voltage ~~of the first operational amplifier~~ and the second reference voltage ~~of the second~~

~~operational amplifier~~.

Claim 9 (original): The semiconductor device of claim 1 wherein the driver and the voltage potential divider are electrically connected to the same voltage source.

Claim 10 (currently amended): The semiconductor device of claim 1 further comprising:

a voltage regulator capable of generating the first voltage source with which the first node of the driver is electrically connected, the voltage regulator comprising:

a PMOS transistor wherein a source of the PMOS transistor is electrically connected with a ~~first~~ third voltage source, and a drain of the PMOS transistor is electrically connected with the first node of the driver; and

a third operational amplifier comprising a first input end, a second input end and an output end electrically connected with the drain of the PMOS transistor, a ~~first~~ third reference voltage and a gate of the PMOS transistor respectively, the third operational amplifier capable of fixing a voltage potential of the drain of the PMOS transistor to a voltage potential of the ~~first~~ third reference voltage.

Claim 11 (currently amended): The semiconductor device of claim 10 further comprising a reference voltage generator capable of generating the first reference voltage ~~of the first operational amplifier~~, the second reference voltage ~~of the second operational amplifier~~ and the ~~first~~ third reference voltage.

Claim 12 (original): The semiconductor device of claim 1 being a flash memory.